

Fig. 1
Prior Art

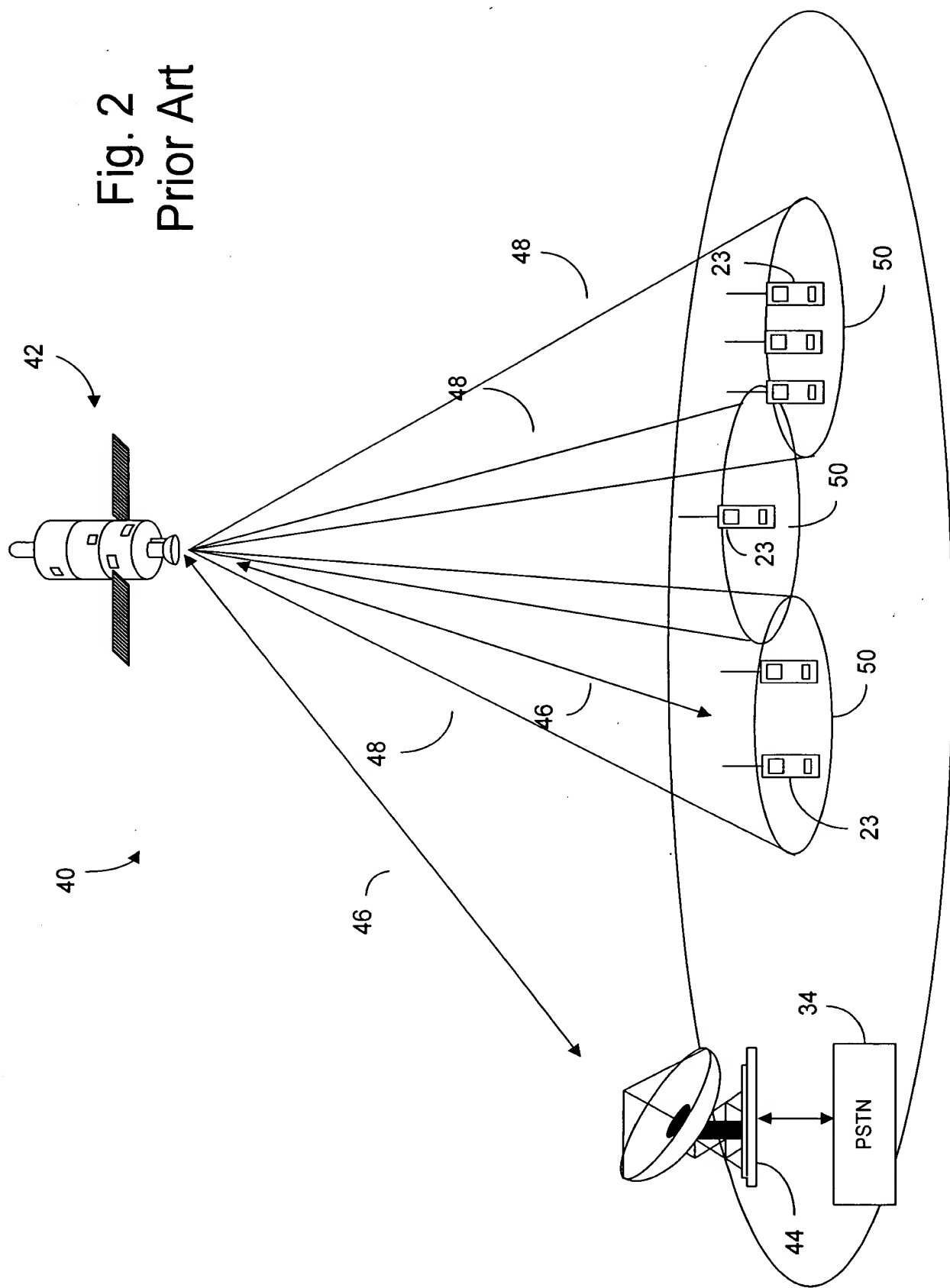


Fig. 2
Prior Art

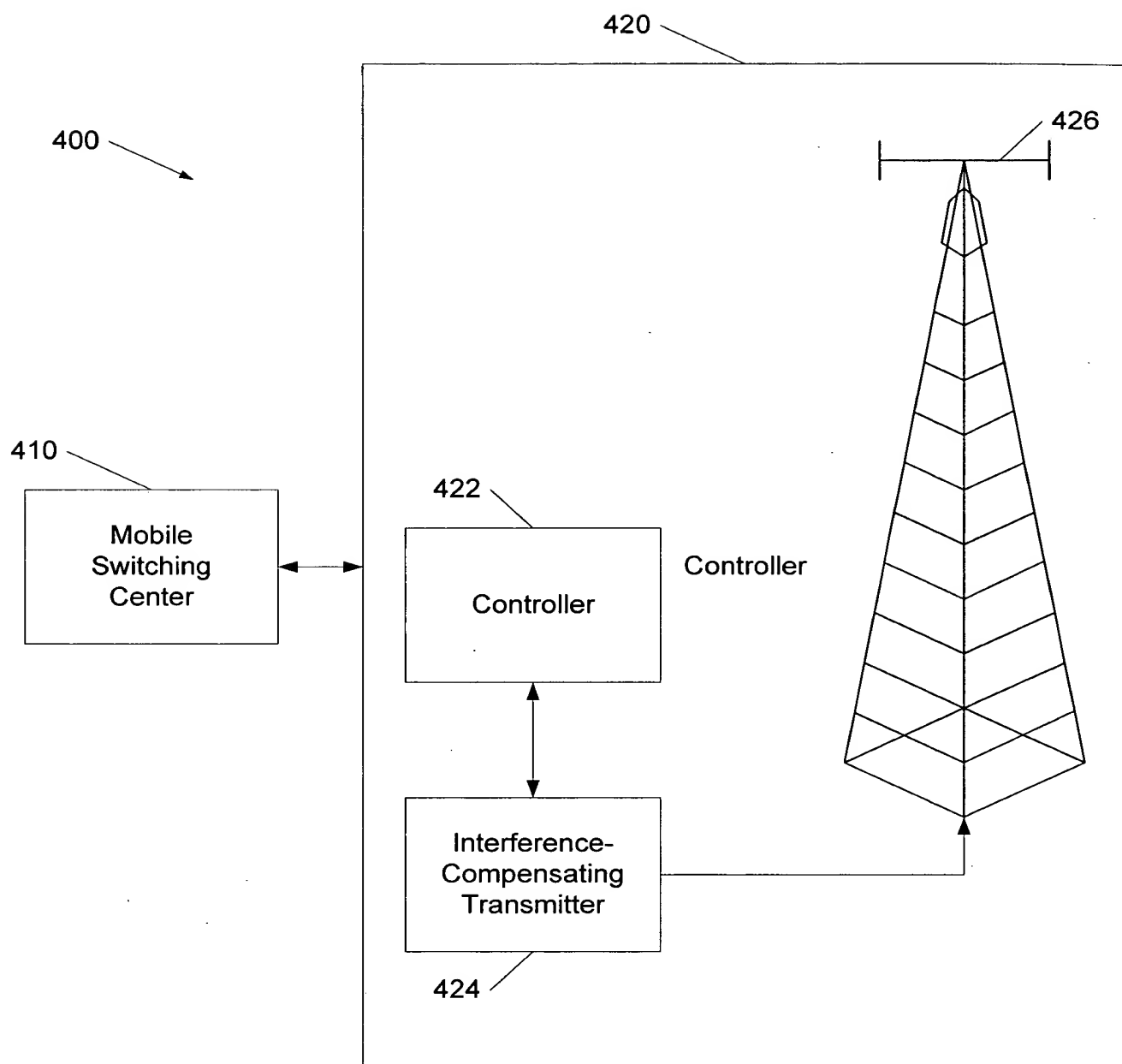


FIG. 4

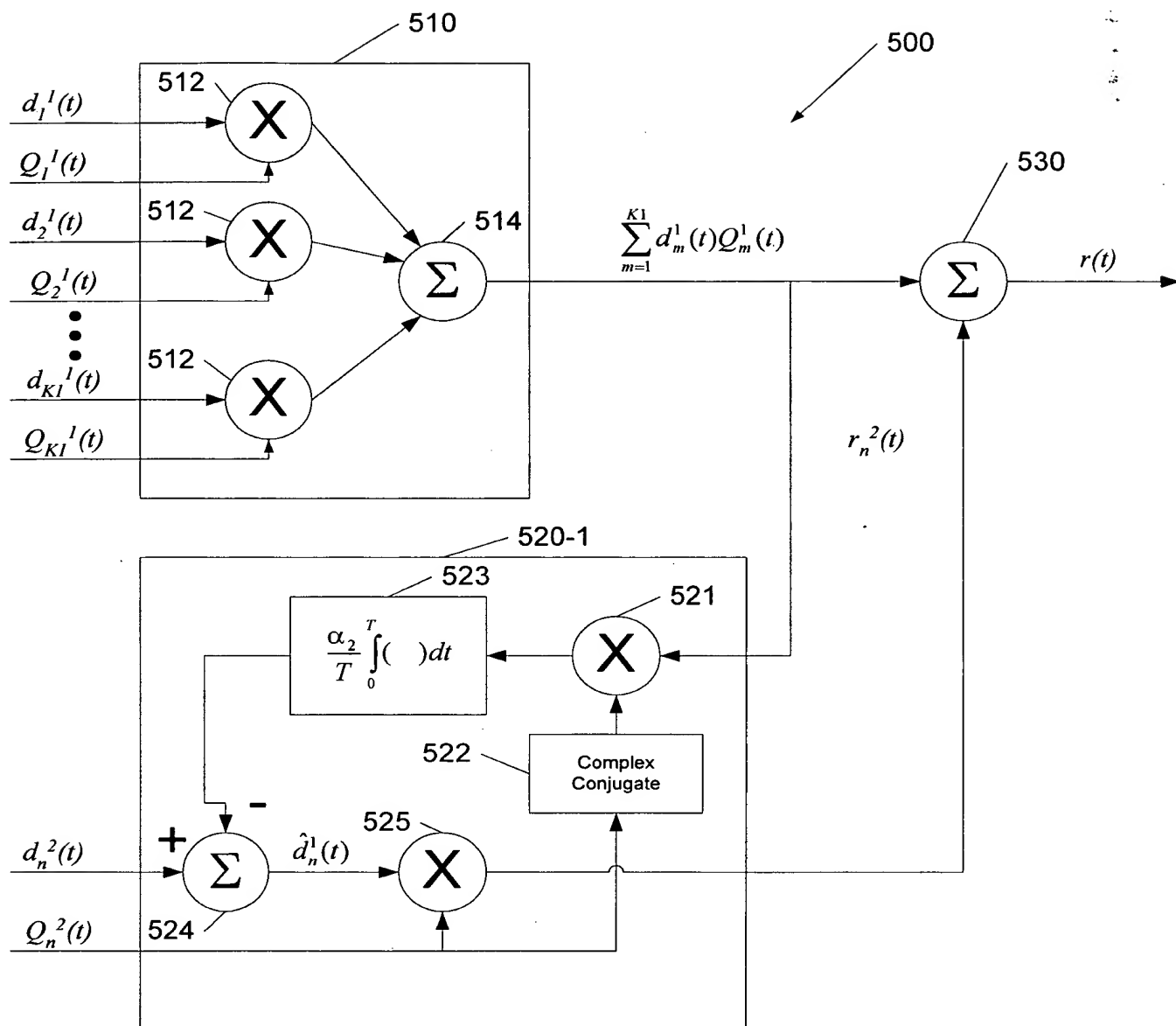


FIG. 5

600

Block diagram of a fourth-order digital filter 520'. The input $d_j^1(t)$ and $Q_j^1(t)$ are fed into a summing junction 524'. The output of 524' is $\hat{d}_j^1(t)$, which is then multiplied by a gain 525. The output of 525 is fed into a "Complex Conjugate" block 522. The output of 522 is fed into three multipliers 521. The inputs to these multipliers are $\sum_{m=1}^{K4} d_m^4 Q_m^4$, $\sum_{m=1}^{K3} d_m^3 Q_m^3$, and $\sum_{m=1}^{K2} d_m^2 Q_m^2$. The outputs of the multipliers 521 are fed into three integrators 523a', 523b', and 523c', which are labeled $\frac{\alpha_2}{T} \int_0^T () dt$. The outputs of the integrators 523a', 523b', and 523c' are fed back into the summing junction 524' with negative signs.

FIG. 7

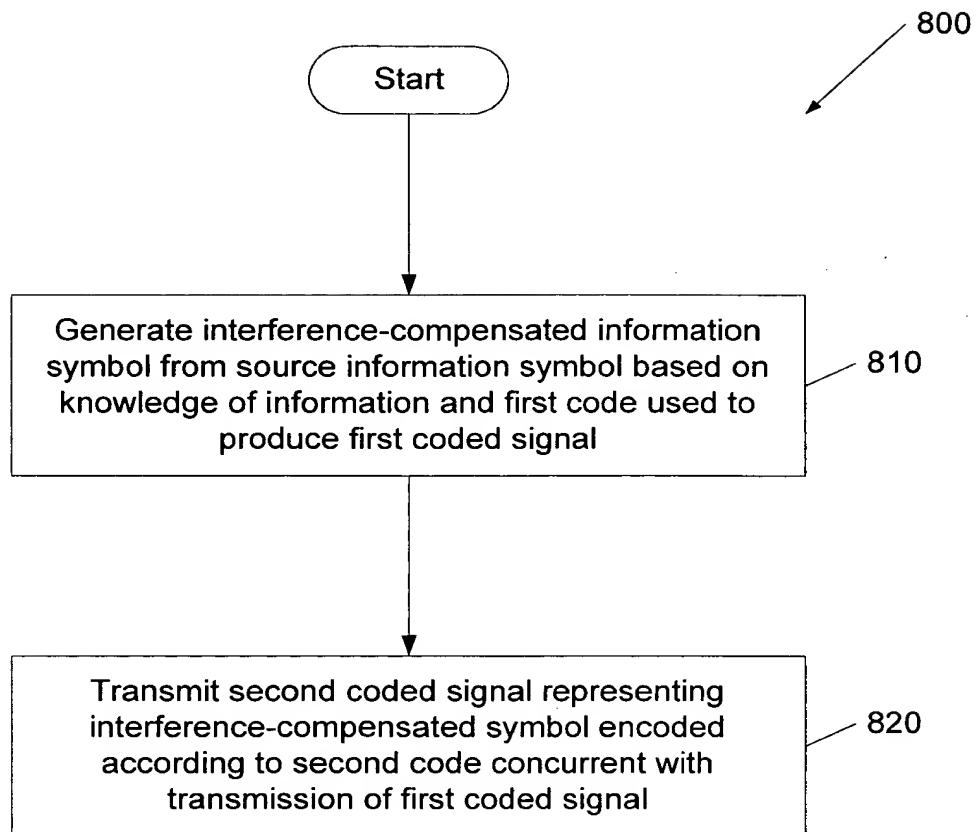


FIG. 8

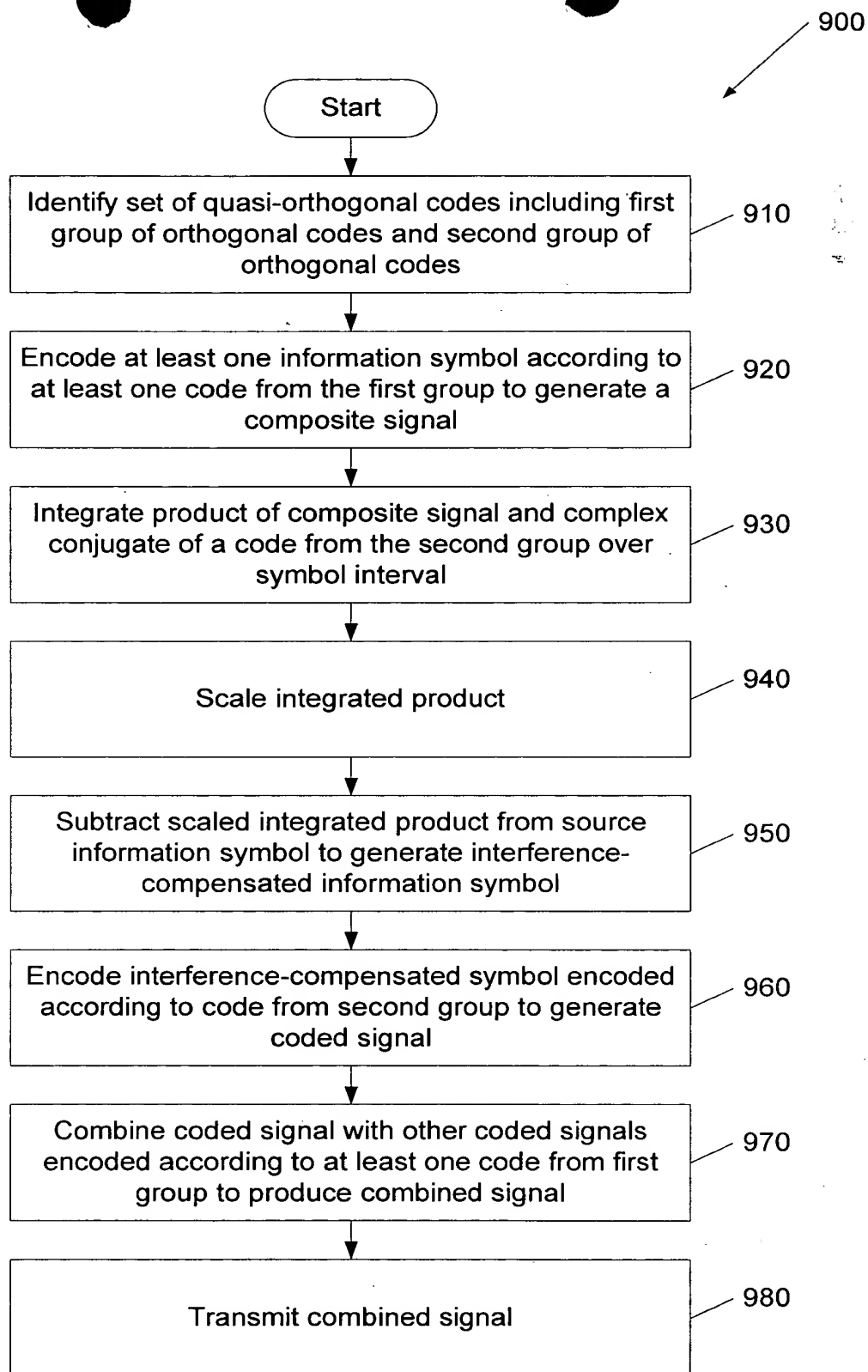


FIG. 9

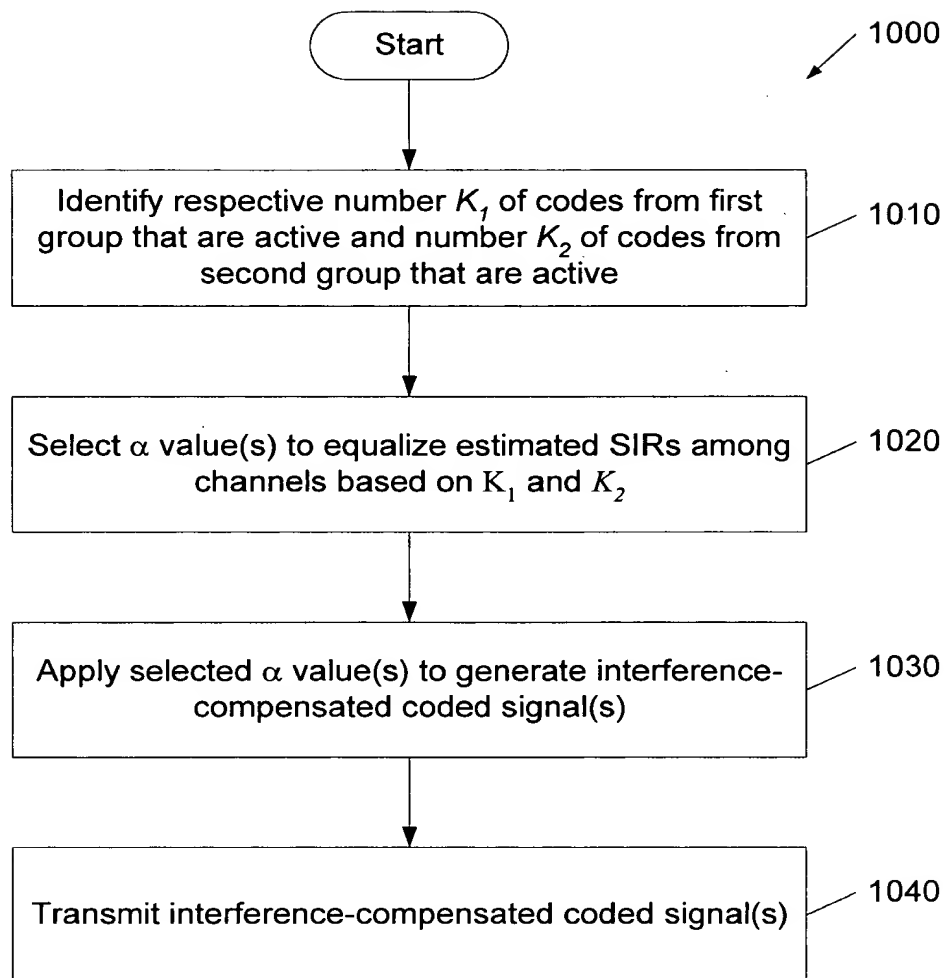


FIG. 10